AMENDMENTS

Please amend the above-identified application as follows:

In the Claims:

This listing of claims replaces all prior versions and listings of claims in the application.

1. (Currently Amended) An apparatus for performing the addition of propagate, kill, and generate recoded numbers, said apparatus comprising:

a circuitry configured to receive at least a first operand, a second operand, and a carry-in bit, the first and second operands comprising respective first and second propagate, kill, and generate recoded number representations of respective first and second binary operands;

a first carry-save adder configured to add said first operand and said second operand to generate a third propagate, kill, and generate recoded number representation and a carry-out bit; and

a modified carry-save adder configured to receive the third propagate, kill, and generate recoded number representation from the first carry-save adder~~, the carry-out bit,~~ and the carry-in bit from the circuitry, add the separate propagate, kill, and generate bits of the third propagate, kill, and generate recoded number representation with the ~~carry-out bit and the~~ carry-in bit to generate a sum value and a carry value, wherein the circuitry provides the carry-out bit from the first carry-save adder at a first output and the carry value from the modified carry-save adder at a second output.

2. (Original) The apparatus of claim 1, wherein said sum value and said carry value are dual rail encoded values.

3-6. (Canceled)

7. (Currently Amended) A method for processing propagate, kill, and generate representations of respective first and second binary operands, comprising:

receiving a carry-in value and a first and a second propagate, kill, and generate representation of respective first and second binary operands;

generating a third propagate, kill, and generate representation and a carry-out value responsive to ~~adding~~ the first and second propagate, kill, and generate representations ~~to generate a third propagate, kill, and generate representation and a carry-out value~~; ~~and~~

~~mathematically~~ logically combining the third propagate, kill, and generate representation with ~~the carry-out value and~~ the carry-in value to generate a sum value and a carry value; and

providing the carry-out value, the carry value, and the sum value as a result of the addition of the first and second propagate, kill, and generate representations.

8. (Currently Amended) The method of claim 7, wherein said step of ~~mathematically~~ logically combining comprises adding the third propagate, kill, and generate representation and the carry-in value.

9. (Canceled)

10. (Currently Amended) The method of claim 7, wherein said step of ~~mathematically~~ logically combining further comprises generating dual rail encoded values.

11-22. (Canceled)

23. (New) The apparatus of claim 1, wherein the sum value is a function of the third propagate representation and the carry-in value.

24. (New) The apparatus of claim 23, wherein the sum value is the XOR combination of the third propagate representation and the carry-in value.

25. (New) The apparatus of claim 1, wherein the carry value is a function of the third propagate representation, the carry-in value, and the third generate representation.

26. (New) The apparatus of claim 25, wherein the carry value is the OR combination of the third generate representation with the AND combination of the third propagate representation and the carry-in value.

27. (New) The apparatus of claim 1, wherein the carry-out value is a function of the first and second generate representations.

28. (New) The apparatus of claim 27, wherein the carry-out value is the OR combination of the first and second generate representations.

29. (New) The apparatus of claim 1, wherein the circuitry provides the sum value at a third output.

30. (New) The method of claim 7, wherein said step of logically combining comprises a XOR combination of the third propagate representation and the carry-in value.

31. (New) The method of claim 7, wherein said step of logically combining comprises an OR combination of the third generate representation with the AND combination of the third propagate representation and the carry-in value.

32. (New) The method of claim 7, wherein said step of generating comprises an OR combination of the first and second generate representations.